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A 16-fs aperture-jitter photonic ADC: 7.0 ENOB at 40 GHz

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Abstract: A photonic ADC based on balanced detection, phase encoded optical sampling, wavelength multiplexing, and electronic quantization is demonstrated. It achieves 7.0 ENOB resolution at a 2GSa/s sub-sampling rate for a 40 GHz input analog signal.

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1. Introduction

Electronic data converters developed over the past 3 years, both in CMOS as well as SiGe platforms, have led to new devices with unprecedented performance. Some notable examples are 65GSa/s CMOS ADC by Fujitsu [1], 40 GSa/s CMOS ADC by Nortel [2], and 40 GSa/s SiGe by RPI [3]. Nonetheless, the overall performance of electronic analog-to-digital (A/D) converters, as defined by the aperture jitter [4], is improving at a rather slow pace. The aperture jitter is the metric that weighs down the resolution, as defined by effective number of bits (ENOB) [4] against the analog bandwidth, and is therefore the key indicator for the speed-resolution performance. Typical ENOB figures of radio frequency (RF) ADCs are about 4.0 for analog frequencies of around 10 to 20 GHz, equivalent to aperture jitter of few hundred femtoseconds (fs). The jitter is due to phase noise limitations of the sampling clock derived from RF synthesizers. It is known, however, that mode-locked lasers exhibit extremely low timing jitter [5] and are potentially ideal candidates for precision sampling.

In this work, by using a mode-locked laser and by combining a phase encoded optical sampling technique [6] with a balanced optical detection scheme, we were able to realize an ADC, that at sub-sampling rate of 2 GSa/s delivers 7.0 ENOB for analog frequencies of up to 40 GHz. It should be noted that recently an alternative optical sampling technique, called photonic time stretch, was used to obtain similar ENOB performance at analog frequency of 10 GHz [7]. Our results show a factor of 4 improvements in terms of analog bandwidth in comparison to that photonic ADC. The equivalent aperture jitter of our ADC is 16 fs, which is to the best of our knowledge one order of magnitude better than any electronic RF (GHz frequencies) A/D converter previously reported.

2. Photonics ADC with balanced detection scheme

Figure 1(a) shows the overall schematic of the ADC system based on optical sampling and wavelength demultiplexing [6][8][9]. In summary, the output of a mode locked laser is sliced into multiple wavelengths channels, which are delayed by different amounts of time and then multiplexed together. The result is a train of pulses that has higher rate than the original laser. This multi-wavelength pulse train is then sent through a modulator where the RF signal of interest is imprinted on it (creating time-wavelength mapping). Later, the wavelength channels are demultiplexed, photodetected, and quantized. The quantizer we use, as in all state-of-the-art high-speed ADCs, operates in differential mode, i.e. it accepts signals that swing from negative to positive voltages around a zero common mode voltage level. However, direct photodetection of either optical output from the Mach-Zehnder (MZ) results in an electrical current signal that is only positive, which means that half of the dynamic range of the electronic ADC will not be exploited. To resolve this, we exploit the fact that complementary outputs of a MZ modulator comprise optical power signals are 180 degrees out of phase. Subtraction of these two positive signals, that share the same common-mode voltage, will result in an output that spans both positive and negative voltages and whose common-mode voltage is set to zero (Figure 1(b)). The subtraction can be best implemented using a balanced photoreceiver whose two input arms are fed by the two complementary outputs of the push-pull MZ modulator. By properly amplifying the resulting dual polarity voltage, it is possible to take advantage of the available full-scale voltage of the electronic ADC, thereby exploiting its full potential. The bipolar nature of the output improves the SNR by 6 dB. This scheme has the added benefit of reducing the number of total required inputs by one-half, as two channels are combined into one. We have successfully implemented this novel detection scheme into our testbed.

3. Experimental results

The testbed created for the ADC demonstration is shown schematically in Figure 1(a). For high-speed sampling, a short linear-cavity laser with ~1.05 GHz repetition rate producing 10 mW output power was used [10]. A commercial 1:8 thin-film filter demultiplexer (JDSU, DWM-2F8DS) with 200 GHz channel spacing and 150 GHz

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bandwidth was used to divide the spectrum into eight channels, and variable time delays (Santec, ODL-330) were used in each channel to impose the required time-frequency map. The channels were then multiplexed into a single path to create a train of pulses with an effective repetition rate that is eight times the original repetition rate. For the experiments here we used only two of the wavelength channels at a time. The pulse train signal was amplified by a 40-dB gain commercial EDFA (MPB R35/130) and passed to a dual-output electro-optic Mach-Zehnder modulator (EOSpace, 40 GHz). Each of the two complementary outputs from the modulator was split into individual wavelength channels with a 1:8 demultiplexer configured to match the demux/mux filter banks at the input. Each channel was detected with a balanced 40 GHz photoreceiver (U2T Photonics, BPRV2125). Post-detection electronics was used to boost the detected pulses to the 1.0 V maximum acceptable peak-to-peak input voltage of the following ADCs. The post-detection electronics consisted of a 3-GHz Gaussian low-pass filter, a DC block, preamplifier (H2 Com 24471, 19-dB gain), DC block, amplifier (Hittite 641, 13-dB gain), and a balun. The electronic ADCs were National Semiconductor ADC10D1000 with two 1 GSa/s differential input channels, operating at 9.0 ENOB, preconfigured on an evaluation board with a Virtex 5 FPGA. The ADCs were synchronously clocked with an RF signal regenerated from the unmodulated optical pulse train using an amplified photodiode, RF filter, and clock distribution circuit (National Semiconductor LMK01000), and the resulting data from the FPGA was post-processed on a computer. Variable optical and RF delay lines were used to precisely align the modulated optical pulse train with the ADC sampling clock. Figure 2 shows the output spectrum of the 2 channel testbed, after interleaving the two 1 GSa/s channels and applying the linearization, according to the principle of phase encoded optical sampling technique [6]. The result is a signal-to-noise-and-distortion ratio (SINAD) of 43.8 dB, equivalent to 7.0 ENOB.

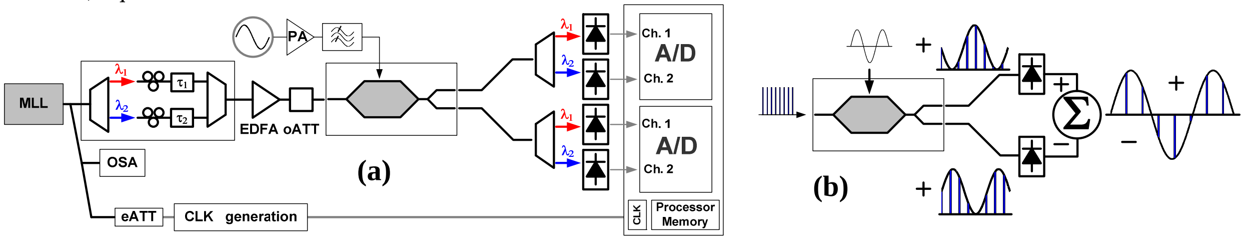

Figure 1 (a) The schematic of the testbed. (b) The balanced detection scheme that creates bipolar output, improving SNR by 6 dB.

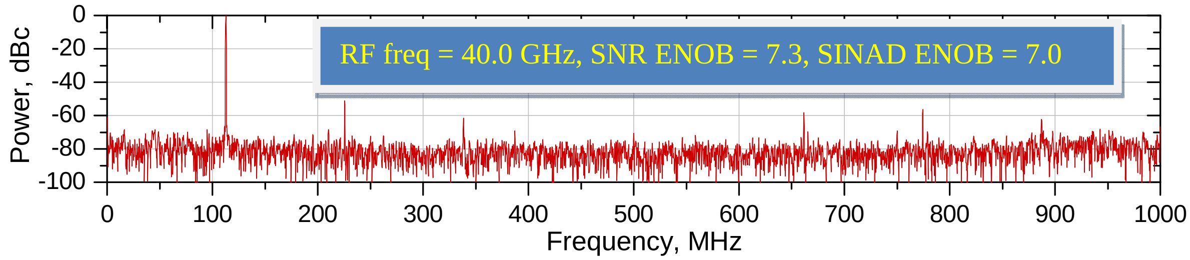

Figure 2 RF spectrum of the subsampled 40 GHz input tone at the rate of 2 GSa/s.

4. Conclusions

We have presented what is to our knowledge the lowest aperture-jitter ADC reported to this date. We have obtained 7.0 ENOB for 40 GHz input analog signals. The sampling rate of 2 GSa/s was obtained by interleaving two 1GSa/s channels. The system is readily scalable to more wavelength channels that will ultimately convert the current subsampling version of the ADC to a Nyquist ADC. Availability of wider bandwidth Mach-Zehnder modulators will directly translate to capability of accepting analog frequencies beyond 40 GHz. Furtheremore, the system is not fundamentally limited to the level of performance demonstrated in this work. Using lower noise detection electronics and exploiting lower jitter mode-locked lasers is expected to lead to even better ENOB values.

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