Polysilicon Surface Micro-Machined Spatial Light Modulator with Novel Electronic Integration

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ABSTRACT

This paper presents a high speed, high resolution phase-only microelectromechanical system (MEMS) spatial light modulator (SLM), integrated with driver electronics, using through-wafer vias and solder bump bonding. It employs a polysilicon thin film MEMS technology that is well-suited to micromirror array fabrication and offers significant improvement in SLM speed in comparison to alternative modulator technologies. Vertical through-wafer interconnections offer scalability required to achieve 1M pixel array size. The design, development, fabrication and characterization of a scalable driver integrated SLM is discussed. Pixel opto-electromechanical performance has been quantified experimentally on prototypes, and results are reported.

INTRODUCTION

Dynamic optical applications require SLMs to have low signal loss, low diffraction, high phase resolution, and a fast response [8]. The primary function of an SLM is to alter the local phase of reflected light, which can be accomplished by deflecting individual mirror pixels up to half the wavelength of the light source. The advantages of SLMs using MEMS technology over Liquid Crystal Displays (LCD) SLMs are a faster response, potentially higher fill factor, and zero polarization effects. Another advantage to MEMS electrostatic actuators is that there is no hysteresis thus facilitating driver control.

The opto-mechanical design of the SLM is based on successful prototype devices already developed by Boston Micromachines Corporation (BMC) and Boston University, with MEMS fabrication performed by Cronos JDS Uniphase. The SLM, as seen in Figure 1, consists of an array of electrostatic parallel-plate actuators that are directly coupled to a segmented membrane mirror through mechanical attachment posts. The actuators are double cantilever, square membranes over fixed electrodes. Each actuator membrane is held at a fixed potential, unlike the electrodes [5]. Cronos JDS Uniphase fabricates the SLM using a three layer, polysilicon, surface micromachining custom process similar to the foundry process: MUMPs®. The thicknesses of the structural and sacrificial layers of a standard MUMPs® process were modified for optimal performance of the SLM. (Table 1.)

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Layer	Use	Thickness (mm)
Thermal Oxide	DRIE Etch Stop	0.1
Low Stress Silicon Nitride	Insulating Layer	1
Polysilicon 0	Address Pads	0.5
Oxide 1	Sacrificial	2.5
Polysilicon 1	Actuators	2
Oxide 2	Sacrificial	2
Polysilicon 2	Mirror	3

Table 1. Layer description and thickness

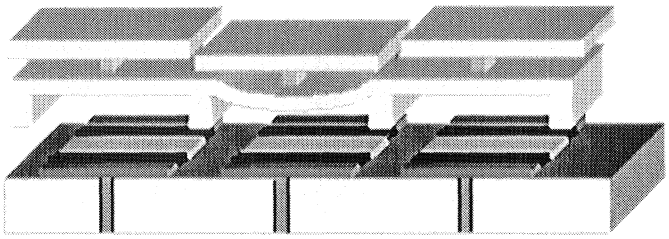

Figure 1. A layered view of an SLM with the split electrodes and vias

Electronic integration of SLMs presents various design and manufacturing challenges such as providing space for interconnections. In order to maximize the area of reflectivity (achieve a high fill factor) the area for on-chip electronic connections is limited. A significant change to earlier μSLMs developed by the project team, is the integration of driver electronics through multi-wafer bump bonding instead of peripheral wire-bonding, allowing for scalability.

Digital and analog control of MEMS arrays offer various benefits and challenges. Analog circuitry is external and cumbersome, due to several wire bonds and complex controls. Non-external analog circuitry is not possible due to power dissipation, and the constrained area (per pixel) necessary to fit a D/A and amplifier. Digital driver electronics have more simplified circuitry and are therefore more compact and batch produced.

DESIGN AND FABRICATION OF SLM

The design specifications for the μSLM include good optical quality (> 95% reflectivity, > 98% fill factor, λ/50 flatness), fast response (10 microseconds step response) and λ/2 deflection (λ=1.55 microns). The approach currently pursued to integrate the μSLM to driver electronics is to individually optimize the μSLM, the driver electronics, and the

through wafer via fabrication. After vias are made on the backside of the SLM, bump bonds will form a junction between the μSLM and electronics.

The figure and finish of the SLM pixel was improved upon by ion-machining and polishing, respectively. Thin film stress gradients are difficult to control during fabrication and result in curvature of the mirror surface. This stress gradient can be modified to result in a flat mirror by a process developed by Boston University: neutral ion machining the mirror surface to induce a stress in the top layer [1]. Finally, chemo-mechanical polishing of the top polysilicon layer was used to reduce surface roughness by 25%, to 10nm [6].

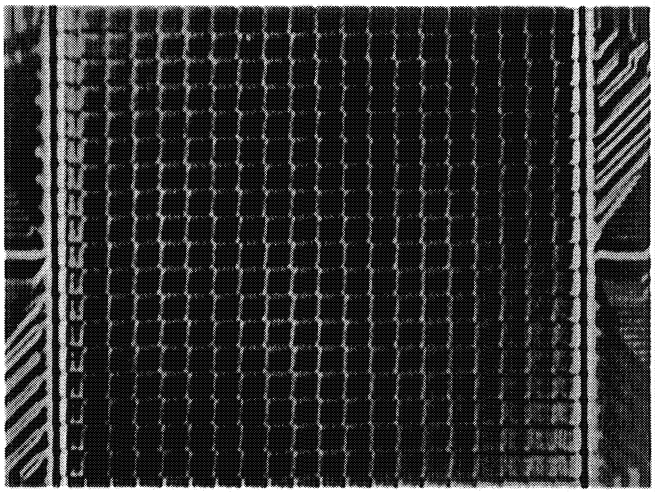

Figure 2. An optical microscope image of a 400 element μ SLM array with 300 microns square pixel.

Good optical quality is determined by high reflectivity, low mirror surface figure, and minimum surface roughness. The as-fabricated silicon has poor reflectivity at the wavelength to be used (λ=1.55μm). To improve this, a metal thin film was deposited onto the mirror surface. This film was deposited after structural release of the devices by e-beam evaporation using a shadow mask. This allowed a thinner metal coating to be deposited, thus minimizing the stress effects on the mirror surface [6].

Technical considerations that must be addressed before integrating the SLM to driver electronics include control of parasitic capacitance, accommodating a digital binary (versus analog) electrostatic driver, and developing a robust-through-wafer etching process. Driver electronics will be implemented for pixels using a 4-bit digital high voltage application specific integrated circuit (ASIC). Consequently the actuator electrode is divided into sub electrodes of geometrically increasing area (as depicted in the schematic layout shown in the Figure 3a). Deep reactive ion etching through the mirror substrate, and back filling of etch holes with conductive vias will provide contacts to the SLM electrodes. Vias, bump bonds, and ASIC contacts are arranged to correspond to electrode locations as seen in Figure 3b.

Designs of the SLM, preliminary via processing and ASIC layout have been completed, as has mirror characterization of test mirror devices.

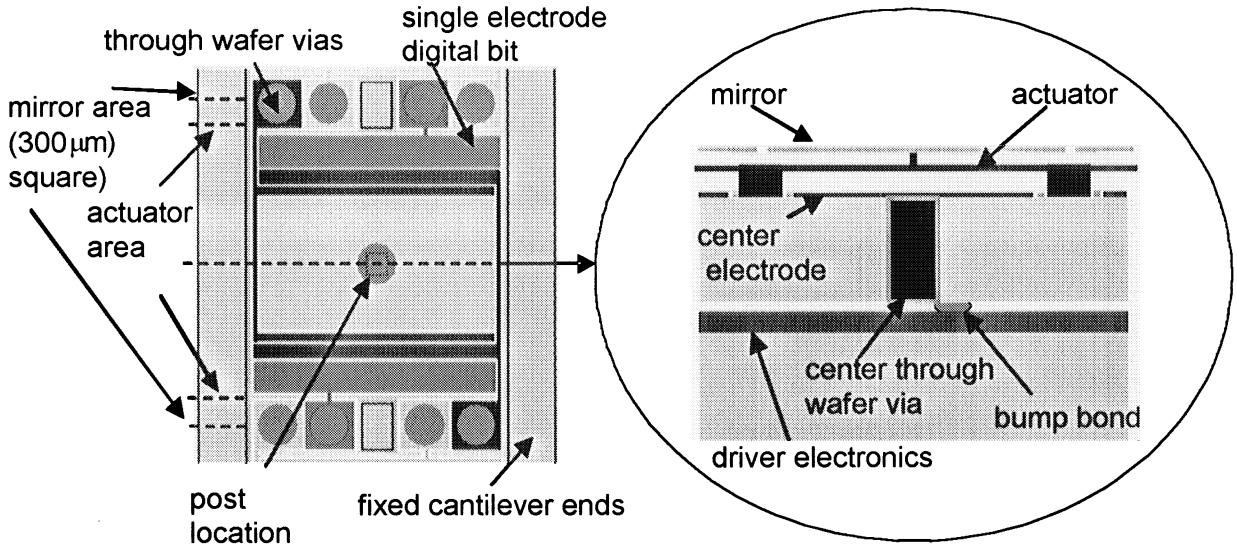

Figure 3a. Top view of 4-bit digital. electrode layout

Figure 3b. Center cross-sectional view of SLM pixel integrated with driver electronics.

RESONANT FREQUENCY CHARACTERIZATION

The effects of squeeze film air damping was investigated. With large plate length to gap thickness ratio, a small displacement of the plate in the normal direction will squeeze air flow out of the device gap through the actuators etch holes and through the cuts of the mirror membrane (which has zero etch holes). The viscosity of the air hampers the flow rate along the gap building a distributed pressure against the actuator and mirror [9].

A test bed (depicted in figure 4) was developed in which the velocity of the μSLM pixel could be measured for pressure varying from 10 mTorr to atmosphere. The test bed consisted of a laser doppler vibrometer (Polytec OFV 303 and 3001) and a custom compact vacuum chamber. The velocity signals (measurable from DC to 250 kHz) were captured and integrated on a computer to obtain displacement. Total deflection was validated using a WYKO.

The electrical inputs of the SLM were two signals: a high voltage signal (140 V) on actuator plane (typically ground) and a low frequency, low voltage (Vpp= 10V) sine wave input on the electrode. Hence, the input varied from 135V to 145V.

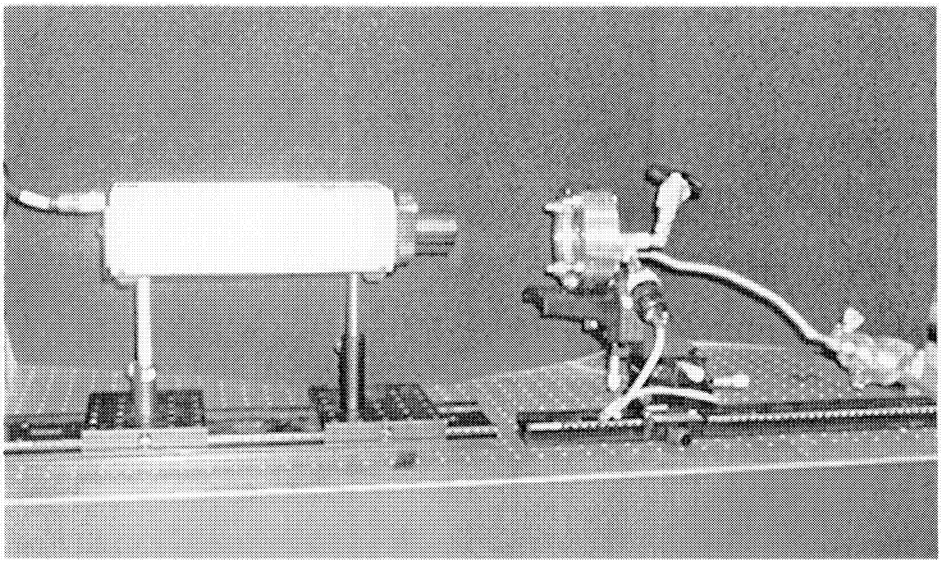

Figure 4. Compact vacuum testing in a vibrometer optical setup

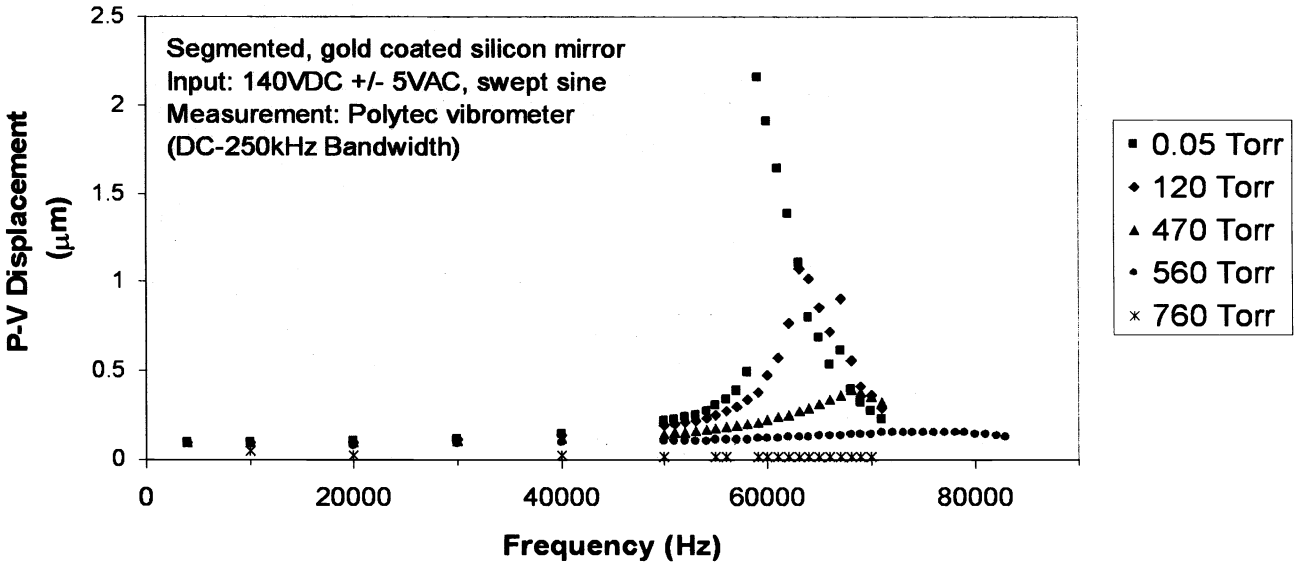

Figure 5. Peak to valley displacement versus the frequency of a sinusoidal input

As seen in figure 5, at atmosphere the device is overdamped; while at pressures below 560 the device is underdamped. The measured underamped resonant frequency (>60 kHz) is of the order of empirical values (76 kHz) which do not take damping into account. The resonant frequency was calculated using the below equations of total mass and spring constant. Note that the spring constant was calculated using experimental data (voltage versus displacement data of the actuator) [2].

$m_{actuator}$ = (density of polysilicon) · (thickness) · (area of the actuator or mirror plate)
m_{total} = m_{mirror}+$m_{actuator}$ (the mass of the whole structure)

$$k = \frac{V^2 A \varepsilon_0}{2x(d-x)^2}$$

$$f = \frac{1}{2 \cdot \pi} \sqrt{\frac{k}{m}}$$

f = 0.76 x 10^5 Hz (Mirror and Actuator) [2]

Another experiment conducted at a fixed pressure (10 mTorr) quantified the effects of a bias voltage. The actuator membrane voltage varied from 0-190 V (voltage bias) while the electrode was at a steady 0.6 Vpp square wave. The data depicted on Figure 6 show that as the voltage bias (which varies in a non linear manner with respect to deflection) increases so does the resonant frequency. Therefore, the resonant frequency is dependent on the stress in the actuator film.

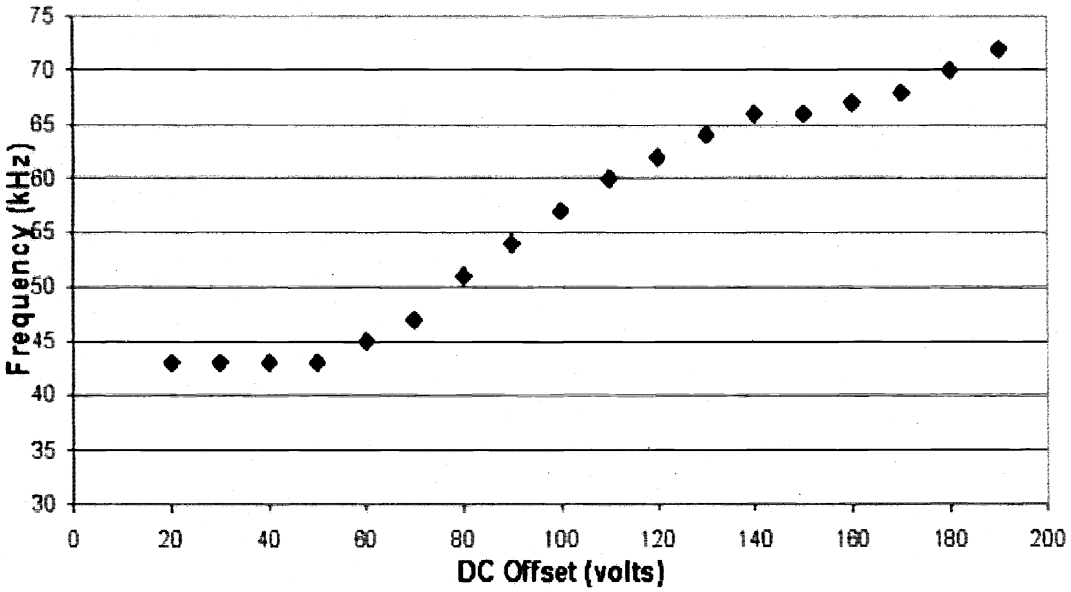

Figure 6. Resonant frequency versus voltage bias at 10 mTorr

The response time results have impacts on the packaging and design of the μSLM. In order to minimize the response time of a μSLM, the packaging environment can be sealed at a low pressure. The voltage bias results suggest that a device with a larger gap would always require a voltage bias and therefore achieve the intended deflections with a faster response time.

ELECTRONIC INTEGRATION

VIAS

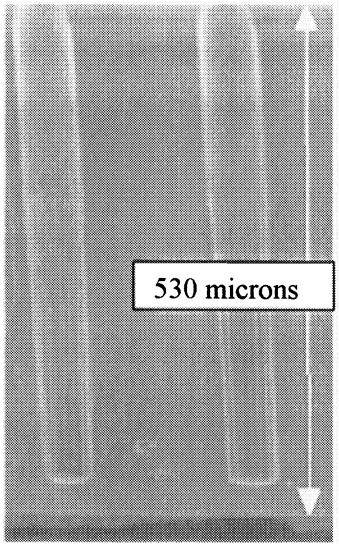

Figure 7. 50 μm through wafer vias achieving 0.5° or less.

Deep reactive ion etching (DRIE) is a particularly attractive approach because high aspect ratio vias, and hence high via densities, are achievable [3]. Adaptive optics applications require ever decreasing electrode sizes, driving the need for small via diameters and higher aspect ratios. In our approach, vias will be implemented after MEMS fabrication is complete, which will present critical alignment, handling, and etch stop challenges. There is also a temperature constraint to the via processing steps, since the SLMs are sensitive to high temperatures processes. Etching processes have to be sensitive to the MEMS.

The vias are formed using the Bosch deep reactive ion etching (DRIE) process at Lawrence Livermore National Laboratory and the Georgia Institute of Technology. The process involves a sequence of backside DRIE of the MEMS substrate, and using hard masks to achieve a 10:1 aspect ratio and 30 micron diameter via. The etch stop is a thin layer of silicon dioxide. Reactive ion etching is performed to punch through the etch stop layers. The substrate hardmask is then stripped and a thermal oxide layer is deposited for via isolation. To form a conductive path, doped polysilicon is deposited. The transparency of the silicon substrate enables via alignment [4]. Via alignment is done using a double-side aligner with optics that look on both sides of the substrate, not an IR aligner.

To increase resolution in piston motion, the electrode area must be divided into smaller segments, resulting in a requirement for smaller diameter vias, implying greater aspect ratios. One solution for smaller vias is to build the SLM onto a wafer having pre-processed vias. Future designs could employ pre-processed vias, a technology which has been demonstrated previously, with a 20 to 1 aspect ratio achieved for a 20 micron diameter via using Deep Reactive Ion Etching on both sides of the wafer [3].

BUMP BONDING

A low parasitic junction between the ASIC and the μSLM will be provided by solder bumps and a wax ring to protect the ASIC from the HF SLM structural release. This task will be accomplished by MicroAssembly Technologies with a bond strength greater than 6.7 ksi. The bumps are low parasitic due to a proprietary low metal and highly conductive bump composition. It will provide a conductive path from electrode to a transistor gate and mechanical mounting to the ASIC, as well as relieve mechanical strain between the two devices.

CONCLUSIONS

The electronic integration of a high performance μSLM presents several design and fabrication challenges. The μSLM, vias, and control electronics have been designed within derived specifications, and for optimal fabrication processes. Using the resonant frequency and optical quality characteristics of the μSLM, performance, processing and packaging have been evaluated.

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